Program: BE Electronics Engineering

Curriculum Scheme: Revised 2012

Examination: Third Year Semester VI

Course Code: EXC 601 and Course Name: VLSI DESIGN

SAMPLE QB

Time: 1 hour Max. Marks: 50

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Note to the students: - All the Questions are compulsory and carry equal marks.

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| Q1. | In CMOS fabrication which type of substrate is used |
| Option A: | P type substrate |
| Option B: | N type substrate |
| Option C: | Can be N type or P type |
| Option D: | T type |
|  |  |
| Q2. | In layout diagram which material is used for gate |
| Option A: | Polysilicon |
| Option B: | Si |
| Option C: | Ge |
| Option D: | GaAs |
|  |  |
| Q3. | The abbreviation designation of input current with low input is |
| Option A: | VIH |
| Option B: | VOH |
| Option C: | VIL |
| Option D: | VOL |
|  |  |
| Q4. | Which parameter is not used in noise margin |
| Option A: | VIH |
| Option B: | VOH |
| Option C: | VIL |
| Option D: | IOL |
|  |  |
| Q5. | In voltage transfer characteristics of MOSFET inverter VIH indicates |
| Option A: | Cut off point |
| Option B: | Critical point |
| Option C: | Saturation point |
| Option D: | Depletion point |
|  |  |
| Q6. | MOSFET stands for |
| Option A: | metal oxide semiconductor field effect transistor |
| Option B: | metal oxide silicon field effect transistor |
| Option C: | Metal semiconductor field effect transistor |
| Option D: | Metal oxygen field effect transistor |
|  |  |
| Q7. | Channel creation is done in |
| Option A: | Accumulation region |
| Option B: | depletion |
| Option C: | Cut off |
| Option D: | inversion |
|  |  |
| Q8. | Correct symbol of CMOS inverter |
| Option A: |  |
| Option B: |  |
| Option C: | CMOS - Wikipedia |
| Option D: | File:CMOS Inverter.svg - Wikimedia Commons |
|  |  |
| Q9. | Channel length modulation parameter is |
| Option A: | λ |
| Option B: | Ω |
| Option C: | Δ |
| Option D: | β |
|  |  |
| Q10. | CCMOS stands for |
| Option A: | Complementary CMOS |
| Option B: | Clocked CMOS |
| Option C: | Control CMOS |
| Option D: | Complementary symmetry CMOS |
|  |  |
| Q11. | In CCMOS logic |
| Option A: | One PMOS & one NMOS with opposite clocks are connected between load & driver |
| Option B: | Only one PMOS transistor is used with gate at ground |
| Option C: | Only one NMOS transistor is used with any input |
| Option D: | Only one NMOS transistor is used gate at ground |
|  |  |
| Q12. | Which logic just pass the signals |
| Option A: | Pass transistor |
| Option B: | Transmission gate |
| Option C: | CPL (complementary pass transistor logic) |
| Option D: | OR gate |
|  |  |
| Q13. | Toggle condition occurs in |
| Option A: | D FF |
| Option B: | T FF |
| Option C: | J K Flip Flop |
| Option D: | S R latch |
|  |  |
| Q14. | Which tree is used in clock distribution |
| Option A: | A |
| Option B: | B |
| Option C: | C |
| Option D: | H |
|  |  |
| Q15. | Zipper is |
| Option A: | Dynamic logic |
| Option B: | Domino logic |
| Option C: | Zipper |
| Option D: | N-P domino logic |
|  |  |
| Q16. | PROM is |
| Option A: | Programmable ROM |
| Option B: | Primary ROM |
| Option C: | Static RAM |
| Option D: | Volatile RAM |
|  |  |
| Q17. | Difference between static & dynamic CMOS |
| Option A: | Both are same |
| Option B: | In static clock is used |
| Option C: | In dynamic logic clock is used |
| Option D: | Extra transistors are used in static RAM |
|  |  |
| Q18. | CMOS behaves like |
| Option A: | AND GATE |
| Option B: | OR |
| Option C: | NOT |
| Option D: | EXOR |
|  |  |
| Q19. | Which architecture is used to design VLSI |
| Option A: | System on device |
| Option B: | Single open circuit |
| Option C: | System on chip |
| Option D: | System on a circuit |
|  |  |
| Q20. | Which provides higher integration density? |
| Option A: | Switch transistor logic |
| Option B: | Transistor buffer logic |
| Option C: | Transistor transistor logic |
| Option D: | System on device |
|  |  |
| Q21. | Charge sharing problem occurs in |
| Option A: | Dynamic logic |
| Option B: | Pseudo logic |
| Option C: | Static |
| Option D: | CCMOS |
|  |  |
| Q22. | RCA vs CLA |
| Option A: | delay of RCA is high |
| Option B: | Delay of CLA is high |
| Option C: | delay of both are same |
| Option D: | there is no delay in RCA |
|  |  |
| Q23. | D flip flop is also called as |
| Option A: | Delay flip flop |
| Option B: | dead flip flop |
| Option C: | deadline flip flop |
| Option D: | Double flip flop |
|  |  |
| Q24. | In realization of Y=A+B how many transitors are required? |
| Option A: | 6 |
| Option B: | 4 |
| Option C: | 5 |
| Option D: | 1 |
|  |  |
| Q25. | In realization of Y=A\*B how many transitors are required? |
| Option A: | 6 |
| Option B: | 4 |
| Option C: | 5 |
| Option D: | 1 |